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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,880	12/20/2001	Ta-Ko Chuang	B-4442 619416-6	4650

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EXAMINER

KILKENNY, TODD J

ART UNIT

PAPER NUMBER

1733

DATE MAILED: 05/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/028,880

Applicant(s)

CHUANG ET AL.

Examiner

Todd J. Kilkenny

Art Unit

1733

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 7 recites the limitation "the other portion" in line 5. There is insufficient antecedent basis for this limitation in the claim. It is unclear what the other portion of the integrated circuit device is. By previously introducing "one portion of the integrated circuit device" and then stating "the other portion of the integrated circuit device" it appears that applicant is attempting to define the integrated circuit device as having two portions. It is unclear what these two portions are and therefore, what "the other portion" refers to.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 7 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura et al (US 5,138,145).

As currently recited, independent claim 7 appears to be broad in scope to the point of reading on conventional underfill chip assemblies. That is, referring to Nakamura et al for example, methods for bonding integrated circuit devices (e.g. a chip) to glass substrate are known to include electrically connecting said chip to said substrate through electrodes (i.e. bonding one portion of the chip to the glass substrate) and thereafter underfilling the chip with a light setting resin (i.e. introducing resin into a gap formed between a portion of the integrated circuit device and the glass substrate), wherein the resin is cured by ultraviolet light (see Figures 5a and 5b; Col. 5, line 58 – Col. 7, line 8).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1 - 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (Specification, page 1, line 14 – page 2, line 8) in view of Kishida et al (US 6,361,867 B2) and Choo et al (US 6,297,869 B1).

Applicant's admitted prior art discloses a conventional method for bonding an integrated circuit device to a glass substrate which includes grinding the edges of a glass substrate via a mechanical grinding device that forms a beveled angle to eliminate sharp edges that can damage the integrated circuit device during bonding (see Figures 1a – 1e). It appears applicant's invention differs from this conventional prior art process

by employing a laser beam to melt the edges of the glass substrate to form the desired beveled (e.g. non sharp edges).

In US 6,361,867 B2, Kishida et al disclose alternative smoothing processes for edges of glass substrates (Figures 2A – 2E; Col. 4, line 43 – Col. 5, line 38; Col. 6, line 1 – Col. 8, line 12).

In the embodiment of Figure 2B, Kishida et al illustrate a smoothing process of mitigating a rough edge surface of a glass substrate thru a heating/melting process to provide the processed edge with a rounded rough surface (Col. 4, lines 53 – 63).

In US 6,297,869 B1, Choo et al teach a method for manufacturing a substrate and a liquid crystal display panel capable of being cut by using a laser. Choo et al teach a grinding step to remove glass chips remaining at edges of the substrate to protect against damage to a printed circuit board attached thereto. Choo et al further disclose as an alternative to a conventional grinder to employ a laser grinder as grinding by laser prevents static charges from generating due to friction on the substrate, which further protects the circuit components on the substrate (Col. 2, lines 5 – 24; Col. 3, lines 14 – 16; Col. 6, lines 50 – 55).

As to claims 1 and 2, it would have been obvious to one of ordinary skill in the art at the time of the invention to substitute the mechanical grinding of the admitted prior art process with a laser provided heating/melting process to smooth the edge of the glass substrate as is alternatively suggested by Kishida et al and Choo et al. One of ordinary skill in the art would have been motivated to employ this alternative approach to avoid

the friction of conventional mechanical grinders and therefore prevent static charges from generating on the substrate as is suggested by Choo et al.

As to claim 3, Choo et al. discloses laser devices comprising first and second lasers, wherein a first laser is employed to cut the substrate and a second laser is employed to ground the edges (Figs. 7 and 8).

As to dependent claims 4 and 5, the integrated circuit device disclosed in the admitted prior art process comprises a driver circuit, a connecting wire, and a protecting circuit connected with an external circuit as claimed by applicant.

8. Claims 7 – 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (Specification, page 1, line 14 – page 2, line 8) in view of Kishida et al (US 6,361,867 B2).

Applicant's admitted prior art discloses a conventional method for bonding an integrated circuit device to a glass substrate which includes grinding the edges of a glass substrate via a mechanical grinding device that forms a beveled angle to eliminate sharp edges that can damage the integrated circuit device during bonding (see Figures 1a – 1e).

In US 6,361,867 B2, Kishida et al disclose alternative smoothing processes for edges of a glass substrate (Figures 2A – 2E; Col. 4, line 43 – Col. 5, line 38; Col.6, line 1 – Col. 8, line 12).

In the embodiment of Figure 2E, Kishida et al suggest a smoothing process incorporating an optical setting resin, wherein at least an edge area of the glass substrate is coated with said resin to form a new smooth edge (Col. 5, lines 29 – 38).

In view of this teaching to Kishida et al, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide a hard resin (e.g. an optical setting resin) coating to the edge of the glass substrate of the admitted prior process to smooth the edge of the glass substrate and sufficiently suppress the rough surface effects of extending cracks.

As to dependent claims 10 and 11, the integrated circuit device disclosed in the admitted prior art process comprises a driver circuit, a connecting wire, and a protecting circuit connected with an external circuit as claimed by applicant.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Todd J. Kilkenny** whose telephone number is (703) 305-6386. The examiner can normally be reached on Mon - Fri (9 - 5).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Ball can be reached on (703) 308-2058. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9310 for regular communications and (703) 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0661.

TJK
April 29, 2003


Michael W. Ball
Supervisory Patent Examiner
Technology Center 1700